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NEW LOW OFFSET APPLICATION SPECIFIC INTEGRATED CIRCUIT

With Hall Cell Sensing Elements for Closed Loop Current Transducers

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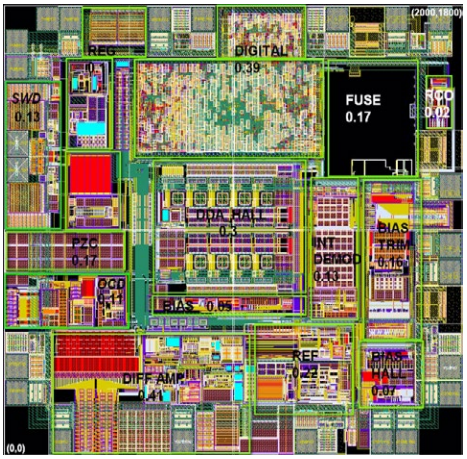
Abstract

Closed loop current transducers using silicon Hall effect devices are used to overcome limitations that exist even in the best open loop current transducers, notably in signal-to-noise ratio, step response time, and temperature drift of sensitivity. The remaining weakness inherent to the architecture of closed loop transducers is their offset when the current to be measured is zero. This paper describes a new Application Specific Integrated Circuit (ASIC) with on-chip Hall sensing elements that use a technique described in a dedicated LEM patent to dramatically improve the offset and offset drift compared to former circuits. The ASIC also includes new features such as a degauss sequence at start-up, over-current detection with a choice of over-range thresholds, and programmability for end-users (see Fig. 1).



Die size 1.8 x 2.0 mm2
CMOS 0.35µm

- 9 Hall cells (8 are active)
- 5K gets for digital block
- 128 fuses as One Time Programmable (OTP) Non Volatile Memory (NVM)

Fig. 1: Picture of the ASIC

Introduction

Figure 2 shows the principle of operation of closedloop current transducers using the magnetic field density induced by the current to be measured into a magnetic core. Hall cells are used in the ASIC as the sensing element to the magnetic field density. This construction has the advantage of isolation from the measured current and a wide frequency range including DC. The Hall cells are made using a standard CMOS process and do not add cost to the ASIC.

For DC and low frequencies (up to a few kHz), the magnetic flux density is sensed by the Hall sensors and a current IS is driven through the secondary winding and a measurement resistor RM to null the flux in a closed-loop arrangement. For higher frequencies, the transducer works as a passive current transformer and IS cancels the flux from IP by the transformer effect. IS can be the output for current output transducers or converted to a voltage output with RM, followed by a voltage amplifier, for voltage output transducers (note the amplifier is not shown in Figure 2).

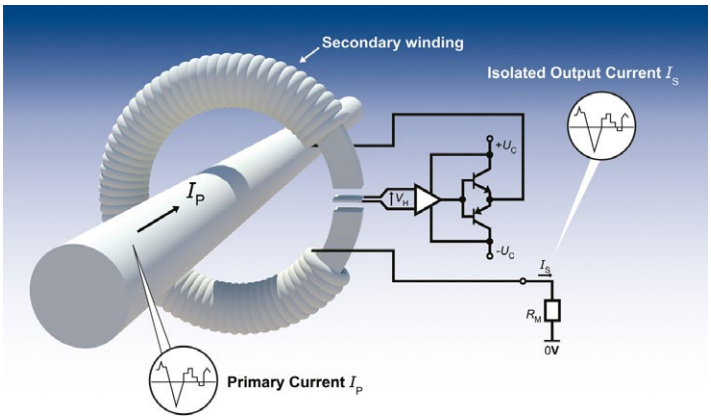


Fig. 2: Closed-Loop Transducer Principle

The exact sensitivity of the Hall cells is not of importance as it is included in the open loop gain that does not contribute to the overall accuracy of the transducer if it is kept high enough.

At frequencies above a few kHz, the secondary current comes directly from the transformer effect. It enables a fast step response that is only limited by the parasitic elements of the coil (resonance frequency) and the voltage amplifier bandwidth. Moreover, noise from Hall cells only contributes to the output noise at frequencies below the transformer effect, while keeping a wide frequency range for the signal. This is the real beauty of the closed loop architecture.

To overcome the offset and 1/f noise of the Hall cells, their output is modulated to a high frequency (1MHz) by biasing the Hall cells successively in two orthogonal

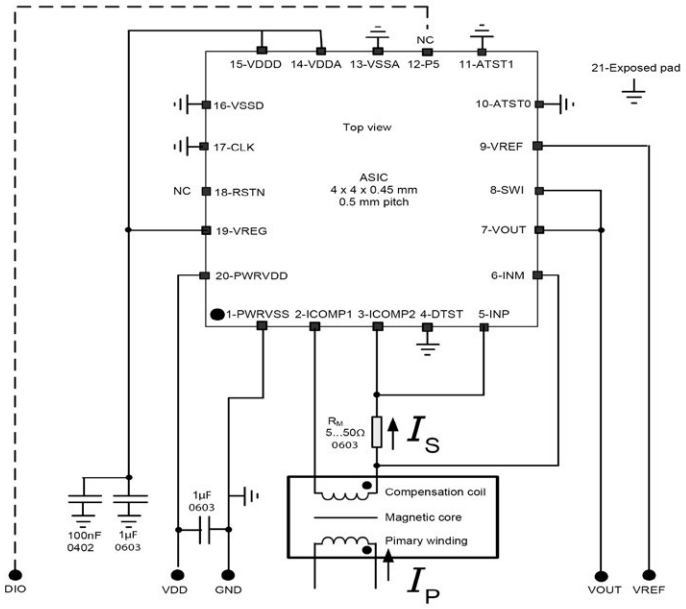


Fig. 3: PCB Schematic for a Standard Voltage Output Closed Loop Transducer

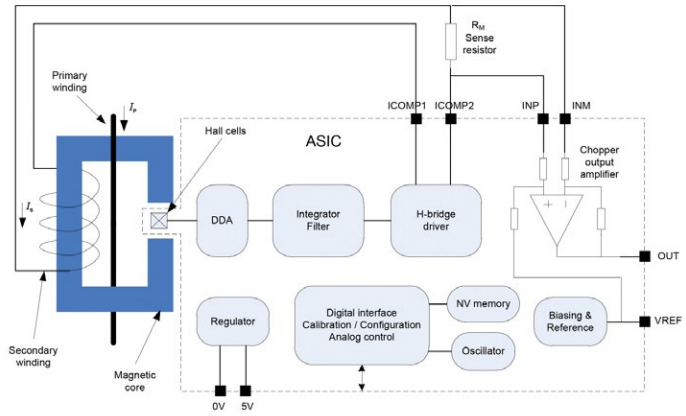


Fig. 4: block diagram of IC

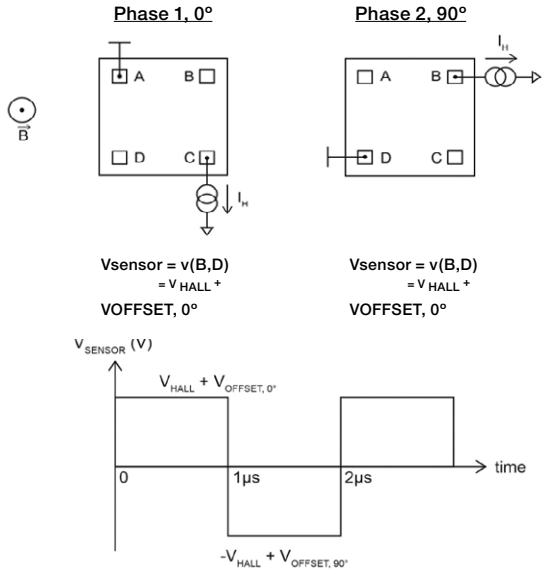


Fig. 5: Spinning Principle

directions (spinning1), and then demodulated after amplification.

The new ASIC described in this paper minimizes the number of electronic components needed to build a voltage output closed loop transducer to only three ceramic capacitors and one sensing resistor. For a current output transducer, the sensing resistor is obviously removed and placed at the end-user side.

If the driver output voltage is not high enough (5V maximum) and/or the output current is too low (150mA maximum), a +/-15V external driver can be used to overcome these limitations. It is mainly used in case of high current measurements (higher than 500A) where the secondary coil current can exceed one amp. This is exactly how it works with the new LF xx10 closed loop Hall effect current transducers using this ASIC.

ASIC architecture

The block diagram of the ASIC is shown in Figure 4.

Eight Hall cells are used to improve the poor signal-to-noise ratio of the sensing element by a factor of √8. The signal increases by a factor of eight whereas the noise increase only by a facto of √8.

Spinning at 1MHz eliminates at first order the Hall cell offset and 1/f noise. Figure 5 describes the well-known principle of the spinning current. It allows the separation of the signal (AC) and the offset (DC) if the offset is the same in the two successive phases. However, this technique has two issues:

- The signal information is in two phases, so there is a delay.
- If, after spinning, the signal is demodulated to its original frequency by a circuit using sampling techniques, there is an aliasing effect on noise.

The offset VOFFSET is then separated from the signal VHALL by the demodulator acting as a high-pass filter.

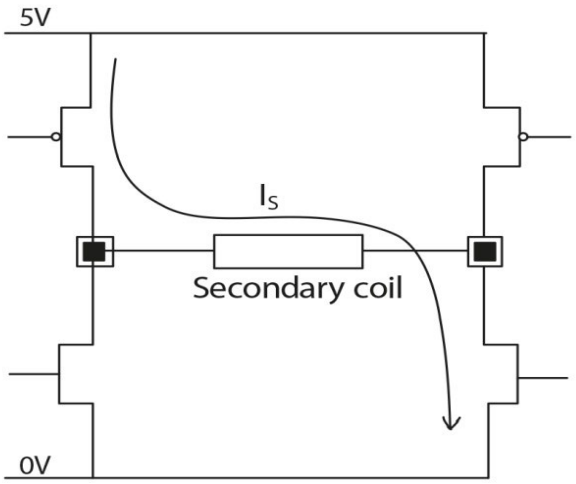


Fig. 6: H-bridge Driver

A differential difference amplifier (DDA) is used to amplify the output of the Hall cells modulated to the spinning frequency (1MHz), before the demodulator/integrator block that is built in a single stage, using switched capacitor architecture. The integrator is the main contributor of the DC open loop gain.

A class-AB driver (H-bridge driver) is used to provide the secondary current up to 150mA with a smooth zero-crossing behavior. Its architecture is based on an H-bridge so the full swing can go up to +/-5V less the voltage drops on the MOS switches (resistance around 5 ohms). It is shown in Figure 6.

A phase correction is mandatory to stabilize the closed loop because two main poles dominate at low frequencies: one due to the coil and one due to the integrator. A pole-zero compensator was therefore added in the loop.

A chopper stabilized amplifier with a fixed gain of four is used to give a low-impedance output after the current-voltage conversion done by the sensing resistor RM. Its offset compared to the output has a standard deviation of 100µV.

In order to be used with different closed-loop topologies, different secondary coils, and air gaps (complete or partial), the integrator time constant and the pole-zero frequency can be configured at LEM.

ASIC programming can be done at LEM and/or by the end-user with fuses. Of course, fuses are only programmable once. A standard UART bus interface is used to communicate with the chip in order to find the optimum configuration and then store it by blowing associated fuses.

New Features Compared to the Previous Generation ASIC Based on Hall Technology (Used in Former Closed Loop Current Transducers Such as the “LTSR” Series Launched in 2003):

- H-bridge (full swing +/-5V) to drive the secondary coil. The previous ASIC was only able to drive +/-2.1V.
- 150 mA drive output current for secondary coil. Previous ASIC was only able to drive 40mA.
- High-accuracy differential output amplifier (class AB): ultra-low offset (100µV standard deviation) and high CMRR (70dB min). The output amplifier offset of the previous ASIC was trimmed with an 8mV step.
- LEM/END-USER configuration with a one-wire digital interface. Not possible with the previous ASIC.
- LEM calibration with the one-wire digital interface. The single calibration that LEM must do is the gain trimming with a 1% step. This allows LEM to avoid a high-accuracy sensing resistor RM although the temperature drift of the resistor is still a contributor to the sensitivity error. Not possible with the previous ASIC.
- Current detection threshold for warning output: thresholds are in the range IPN to 5*IPN with a 0.25*IPN step. Not available in the previous ASIC.
- Built-in degauss function with ability to have a degauss sequence at start up in order to remove initial offset due to magnetization. Not available in the previous ASIC.
- UC = 5V +/-5% or 3.3V +/-5%. The previous ASIC was powered with +5V only.
- Individual device ID: wafer number, XY position on the wafer for traceability, access to the related data log. Not available in the previous ASIC generation.
- Reference voltage may be output or input. The reference voltage output can be 0.5V, 1.65V or 2.5V; reference voltage input range can be from 0.5V to 2.75V. The accuracy of the reference voltage output at 25°C is +/-5mV. The previous ASIC had only a 2.5V reference output with +/-25mV offset and an allowed reference voltage input range from 1.9 to 2.7V.
- Integrator time constant and zero-compensation frequency value are programmed at LEM with the fuse bank. It is set by selecting the wanted value with an external capacitor and resistor on previous ASIC.

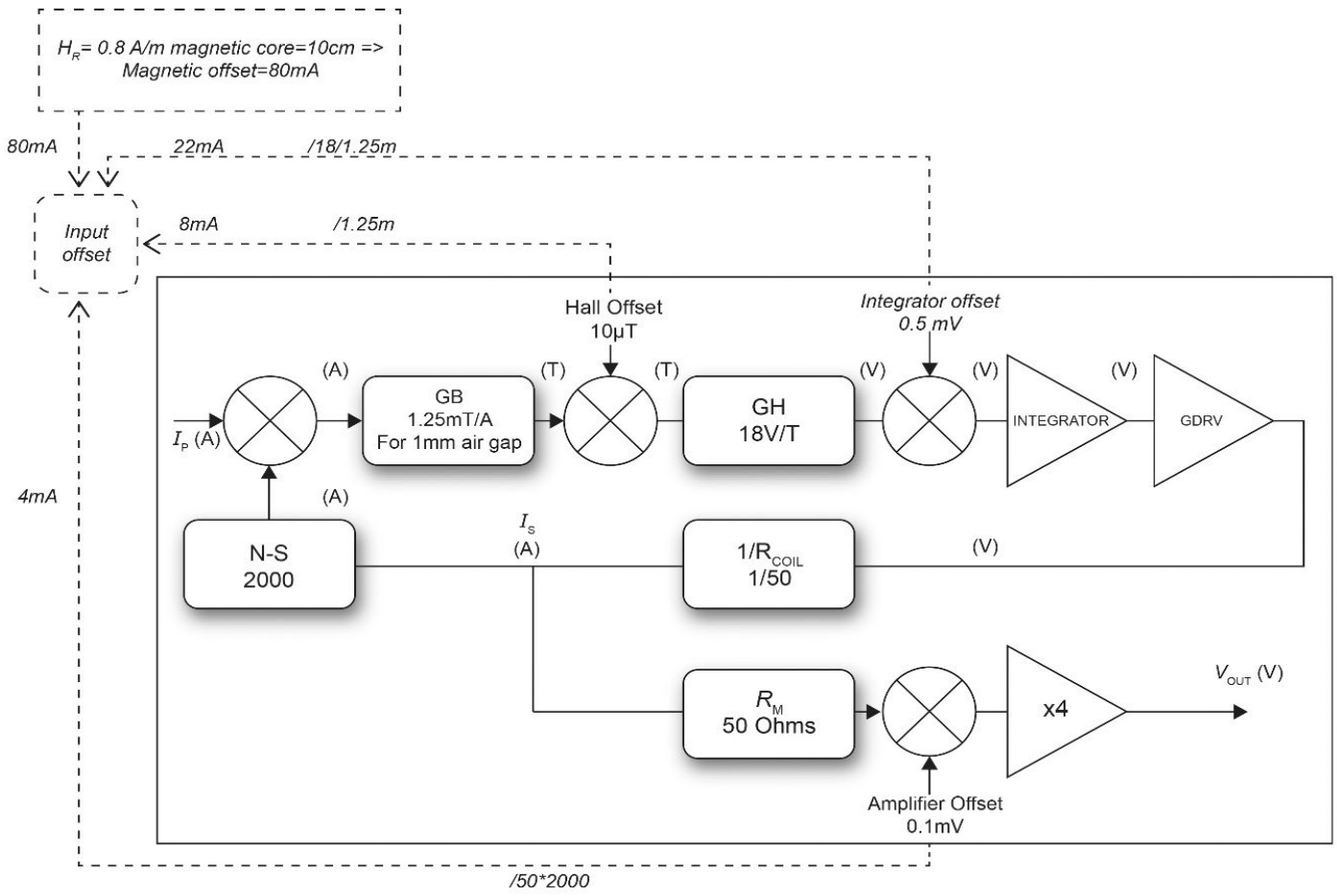


Fig. 7: Closed Loop Model in DC Operation

Offset Performance and the Associated LEM Patent

Compared to the previous generation, the offset and its temperature drift have been improved. The current output offset is always lower than 30µT with a temperature drift lower than 0.3 µT/deg. For a voltage output transducer, the 0.1mV offset of the out-of-the-loop amplifier contributes to the total offset. This offset is four times less than in the previous ASIC.

Figure 7 shows the closed loop in DC signal conditions with the calculation of the offset contributors before trimming.

Annotations:

- GB is the magnetic sensitivity due to the air gap. It is inversely proportional to the width of the air gap.
- GH is the sensitivity gain, including the Hall cell sensitivity and the DDA gain.
- N-S is the number of turns of the secondary coil.
- RCOIL is the resistance of the secondary coil.
- GDRV is the fixed gain of the output driver (=3).

The Hall cell offset is very low (a few µT) due to a proprietary topology that is protected by a LEM patent. The unique design fragments the Hall device into multiple Hall blocks, distributed over the silicon area and easily interconnected to improve the effectiveness of the spinning technology.

The fragmentation allows splitting the offset of the Hall cell in small levels more effectively, cancelled by the spinning technique. The spinning completely cancels offsets in the linear system. However, Hall cells cannot be seen as linear, so some residual offset remains. Non-linearity increases with the bias voltage level. A low Hall bias voltage minimizes offsets and offsets drifts. However, reducing the bias voltage degrades the signal-to-noise ratio. To recover signal-to-noise ratio, an array of Hall cells are used, with each cell being weakly biased.

Historically, the challenge has been integrating the array of Hall cells easily without layout limitations, while keeping the geometric symmetry. The use of a DDA Differential difference amplifier topology has been a great contributor to overcoming this.

The output of the circuit is proportional to the sum of the differential inputs (see Figure 3). The overall secondary current offset is trimmed by the silicon foundry and stored in a fuse bank. The offset of the output amplifier does not need trimming.

Package

The ASIC is packaged in a thin 4x4mm QFN. The thickness of the package is 0.45mm with a worst case of 0.5mm so a thin air gap can be used to reduce the offset and improve the signal-to-noise ratio.

Figure 8 shows the top and bottom of the ASIC package.

The third line indicates the qualification level (ES stands for Engineering Sample, IND for Industrial grade, AUT for automotive grade) and the LEM version (A).
The fourth line YYWWIZZ gives the date code (YY: year; WW: week; I: plant identification; ZZ: reserved for the assembly line).

Quality Level

The qualification of the ASIC includes all tests described in the automotive standard AEC Q100: visual inspection, ESD, Latch-Up, temperature cycling, and aging 1000 hours at 125°C with 85% relative humidity.

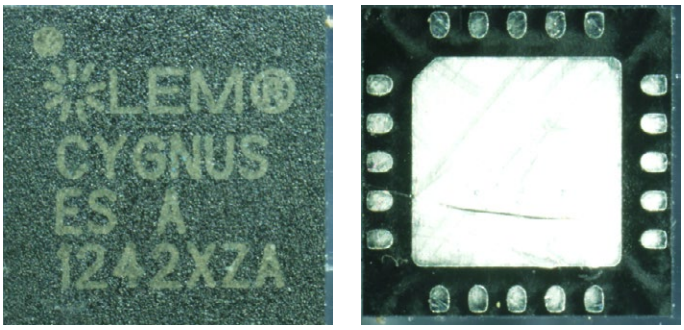


Fig. 8: ASIC QFN Package

Conclusion

A new Application Specific Integrated Circuit for closed loop current transducers has been presented whose performance has been improved, especially the offset and temperature drift. Furthermore, additional features such as degauss function and over-current detection with adjustable threshold levels have been included in the new ASIC.

For further performance improvement, it would be necessary to consider more costly technologies such as those based on fluxgate sensors, which have a better signal-to-noise ratio than the Hall cells in the ASIC described in this paper.

This new ASIC has been used for the first time in the new LF xx10 current transducers series precisely to improve the accuracy level, especially across temperature ranges, due to its superior offset drift. This new range of closed loop current transducers includes models for 200, 300, 500, 1000 and 2000 A nominal, providing a full new range of devices to serve the demanding world of high-performance power electronics and their applications.

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